Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 1, 9, 15, 21, 23, and 37 as follows:

Please cancel claims 7, 8, 21, 22, and 29-36 without prejudice.

1. (currently amended): An apparatus for the two cycle computation of a plurality of types of complex multiplication, the apparatus comprising:

a first storage means for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

multiplier means for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

a second storage means for storing products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

adder means for simultaneously performing additions and subtractions in a second cycle of operation to produce real result (Xr*Yr)-(Xi*Yi) and imaginary result (Xr*Yi)+(Xi*Yr) if the type of complex multiplication being performed is a nonconjugated operation ~~is being performed~~, said adder means further for operating to simultaneously perform~~ing~~ additions and subtractions in the second cycle of operation to produce real result (Xr*Yr)+(Xi*Yi) and imaginary result (Xi*Yr)-(Xr*Yi) if the type of complex multiplication being performed is a conjugated operation ~~is being performed~~;

a multiplexer coupled to the multiplier means and the adder means, said multiplexer selecting which produced products are added to or subtracted from each other based on the type of complex multiplication being performed; and

a third storage means for storing the results of said adder means.

2. (original): The apparatus of claim 1 further comprising:

accumulator means for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder means with the current contents of said third storage means,

wherein said third storage means is further for storing the results of said accumulator means.

3. (original): The apparatus of claim 2 further comprising:

extended precision storage means,

wherein said accumulator means is further for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder means with both the current contents of said third storage means and the current contents of said extended precision storage means,

wherein said extended precision storage means is for storing extended precision results of said accumulator means.

4. (original): The apparatus of claim 3 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

5. (original): The apparatus of claim 1 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

6. (original): The apparatus of claim 1 wherein multiplier means is further for simultaneously performing multiplications in the second cycle of operation utilizing a second pair of operands.

Claims 7-8 (canceled)

9. (currently amended): A two cycle method ~~of~~for performing a plurality of types of complex multiplication of a first complex operand and a second complex operand stored in a first memory device, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi, the method comprising the steps of:

performing simultaneous multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

storing products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi in a second memory device in the first cycle of operation;

selecting which stored products are added to or subtracted from each other based on a type of complex multiplication;

performing simultaneous additions and subtractions in a second cycle of operation to produce real result (Xr*Yr)-(Xi*Yi) and imaginary result (Xr*Yi)+(Xi*Yr), if the type of complex multiplication being performed is a nonconjugated operation ~~is being performed~~;

performing simultaneous additions and subtractions in the second cycle of operation to produce real result (Xr*Yr)+(Xi*Yi) and imaginary result (Xi*Yr)-(Xr*Yi), if the type of complex multiplication being performed is a conjugated operation ~~is being performed~~; and

storing the real and imaginary results of the additions and subtractions in a third memory device in the second cycle of operation.

10. (original): The method of claim 9 further comprising, before the step of storing the real and imaginary results, the step of:

performing accumulations in the second cycle of operation to accumulate the results of the additions and subtractions with the current contents of the third memory device.

11. (original): The method of claim 9 further comprising, before the step of storing the real and imaginary results, the step of:

performing accumulations in the second cycle of operation to accumulate the results of the additions and subtractions with both the current contents of the third memory device and the contents of an extended precision register.

12. (original): The method of claim 11 further comprising the step of:

storing the extended precision accumulated result in the extended precision register.

13. (original): The method of claim 11 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

14. (original): The method of claim 9 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

15. (currently amended): An apparatus for the single cycle computation ~~of~~ for a plurality of types of complex multiplication, the apparatus comprising:

a first storage means for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

multiplier means for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

adder means for simultaneously performing additions and subtractions in the first cycle of operation to produce real result (Xr*Yr)-(Xi*Yi) and imaginary result (Xr*Yi)+(Xi*Yr) if the type of complex multiplication being performed is a nonconjugated operation ~~is being performed~~, said adder means further for simultaneously performing additions and subtractions in the first cycle of operation to produce real result (Xr*Yr)+(Xi*Yi) and imaginary result (Xi*Yr)-(Xr*Yi) if the type of complex multiplication being performed is a conjugated operation ~~is being performed~~;

a multiplexer coupled to the multiplier means and the adder means, said multiplexer selecting which produced products are added to or substracted from each other based on the type of complex multiplication being performed; and

a third storage means for storing the results of said adder means.

16. (original): The apparatus of claim 15 further comprising:

accumulator means for simultaneously performing accumulation in the first cycle of operation to accumulate the results of said adder means with the current contents of said third storage means,

wherein said third storage means is further for storing the results of said accumulator means.

17. (original): The apparatus of claim 16 further comprising:

extended precision storage means,

wherein said accumulator means is further for simultaneously performing accumulation in the first cycle of operation to accumulate the results of said adder means with both the current contents of said third storage means and the current contents of said extended precision storage means,

wherein said extended precision storage means is for storing extended precision results of said accumulator means.

18. (original): The apparatus of claim 17 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

19. (original): The apparatus of claim 15 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

20. (original): The apparatus of claim 15 wherein multiplier means is further for simultaneously performing multiplications in the second cycle of operation utilizing a second pair of operands.

21. (currently amended): An apparatus for the single cycle computation of a plurality of types of complex multiplication, the apparatus comprising:

a first storage means for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

multiplier means for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

a second storage means; ~~and~~

adder/accumulator means for simultaneously performing additions and subtractions in the first cycle of operation to produce real result (Xr*Yr)-(Xi*Yi) and imaginary result (Xr*Yi)+(Xi*Yr) if the type of complex multiplication being performed is a nonconjugated operation ~~is being performed~~, said adder/accumulator means further for simultaneously performing additions and subtractions in the first cycle of operation to produce real result (Xr*Yr)+(Xi*Yi) and imaginary result (Xi*Yr)-(Xr*Yi) if the type of complex multiplication

being performed is a conjugated operation ~~is being performed~~, said adder/accumulator means is further for simultaneously performing accumulation in the second cycle of operation to accumulate the results with the current contents of said second storage means,

wherein said second storage means is further for storing the accumulated results of said adder/accumulator means; and

a logical array coupled to the multiplier means and the adder/accumulator means, said logical array aligning the produced products to determine which produced products are added to or subtracted from each other based on the type of complex multiplication being performed.

22. (original): The apparatus of claim 21 further comprising:

extended precision storage means,

wherein said adder/accumulator means is further for simultaneously performing accumulation in the first cycle of operation to accumulate the results of said adder means with both the current contents of said second storage means and the current contents of said extended precision storage means,

wherein said extended precision storage means is for storing extended precision results of said adder/accumulator means.

23. (currently amended): A single cycle method ~~o~~for performing a plurality of types of complex multiplication of a first complex operand and a second complex operand stored in a first memory device, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi, the method comprising the steps of:

performing simultaneous multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

storing products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi in a second memory device in the first cycle of operation;

aligning the stored products to determine which stored products are added to or subtracted from each other based on a type of complex multiplication being performed;

performing simultaneous additions and subtractions in the first cycle of operation to produce real result (Xr*Yr)-(Xi*Yi) and imaginary result (Xr*Yi)+(Xi*Yr), if the type of complex multiplication being performed is a nonconjugated operation ~~is being performed~~;

performing simultaneous additions and subtractions in the first cycle of operation to produce real result (Xr*Yr)+(Xi*Yi) and imaginary result (Xi*Yr)-(Xr*Yi), if the type of complex multiplication being performed is a conjugated operation ~~is being performed~~; and

storing the real and imaginary results of the additions and subtractions in a second memory device in the first cycle of operation.

24. (original): The method of claim 23 further comprising, before the step of storing the real and imaginary results, the step of:

performing accumulations in the first of operation to accumulate the results of the additions and subtractions with the current contents of the second memory device.

25. (original): The method of claim 23 further comprising, before the step of storing the real and imaginary results, the step of:

performing accumulations in the first cycle of operation to accumulate the results of the additions and subtractions with both the current contents of the second memory device and the contents of an extended precision register.

26. (original): The method of claim 25 further comprising the step of:

storing the extended precision accumulated result in the extended precision register.

27. (original): The method of claim 25 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

28. (original): The method of claim 23 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

Claims 29-36 (canceled)

37. (currently amended): An apparatus for the two cycle computation of a plurality of complex multiplication, the apparatus comprising:

a first storage register for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

a multiplier for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

a second storage register for storing products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

an adder for simultaneously performing additions and subtractions in a second cycle of operation to produce real result (Xr*Yr)-(Xi*Yi) and imaginary result (Xr*Yi)+(Xi*Yr) if a type of complex multiplication being performed is a nonconjugated operation ~~is being performed~~, said adder means further for simultaneously performing additions and subtractions in the second cycle of operation to produce real result (Xr*Yr)+(Xi*Yi) and imaginary result (Xi*Yr)-(Xr*Yi) if the type of complex multiplication being performed is a conjugated operation ~~is being performed~~;

a multiplexer coupled to the multiplier and the adder, said multiplexer selecting which produced products are added to or subtracted from each other based on the type of complex multiplication being performed; and

a third storage register for storing the results of said adder means.

38. (original): The apparatus of claim 37 further comprising:

an accumulator for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder with the current contents of said third storage register,

wherein said third storage register is further for storing the results of said accumulator.

39. (original): The apparatus of claim 38 further comprising:

an extended precision storage register,

wherein said accumulator is further for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder with both the current contents of said third storage register and the current contents of said extended precision storage means,

wherein said extended precision storage register is for storing extended precision results of said accumulator.

40. (original): The apparatus of claim 39 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

41. (original): The apparatus of claim 37 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.